REPORT DOCUMENTATION PAGE

AFRL-SR-BL-TR-98-
0679

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
		Final 01 Jul 95 to 30 Jun 98

4. TITLE AND SUBTITLE
Photonic ATM Front End Processors

5. FUNDING NUMBERS
61101E
C406/03

6. AUTHOR(S)
Professor Choa

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of Maryland
Baltimore County
1000 Hilltop Circle
Baltimore MD 21250

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NE
110 Duncan Avenue RmB115
Bolling AFB DC 20332-8030

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
F49620-95-1-0446

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION AVAILABILITY STATEMENT
APPROVAL FOR PUBLIC RELEASED;DISTRIBUTION UNLIMITED

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

In this work, we have built 3 control circuit boards running at 2.5 Gb/s. These include a cell delineation circuit borad, a VCI over-writing circuit board, and a cell synchronizer control circuit board, and a cell synchronizer control circuit board. We also design and fabricate an 1x2 semiconductor optical amplifier (SOA) broadband space switch. Multiwavelength-signal switching using the fabricated switches is demonstrated. We also build the VCI overwriting and cell synchronization optical systems using both LiNbO3 switches and the fabricated switches. We have completed the interfaces of the optical systems with the control circuit boards and finally demonstrated the proposed photonic ATM front-end processor at 2.5 Gb/s.

14. SUBJECT TERMS			15. NUMBER OF PAGES
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

1998

FINAL REPORT

PHOTONIC ATM FRONT END PROCESSORS

Professor F. S. Paul Choa

Department of Computer Science and Electrical Engineering
University of Maryland Baltimore County
Baltimore, MD 21250
Tel: 410-455-3272
Fax: 410-455-6500
e-mail choa@umbc.edu

and

Professor H. Jonathan Chao

Department of Electrical Engineering
Polytechnic University
Brooklin, NY 11201
Tel: 718-260-3302
Fax: 718-260-3074
e-mail chao@antioch.poly.edu

Grant Number: F49620-95-1-0446

Attention: Dr. Alan Graig AFOSR
Dr. Robert Leheny DARPA

CC. Dr. Bert Hui DARPA

SUMMARY

The objective of this research work is to build a photonic ATM front end processor including the functions of cell delineation, virtual channel identifier (VCI) over-writing, and cell synchronization and for future photonic ATM/IP switches.

Optical networking technology has well progressed in the past few years. The wavelength-division-multiplexing (WDM) technology prevails all over the world due to the advantages of bringing a huge capacity to existing optical networks without installing new fibers. Recent development on photonic add/drop multiplexers and reconfigurable photonic switches can further facilitate the optical networking. Compared with using electronic switches, they can handle the traffics in a network more conveniently and cost effectively. All optical networking concept is now well accepted by all carriers including even the most conservative carriers like MCI-Worldcom. Recently, due to the growth of internet, the research topics has further moved toward trying to remove the SONET layer out of the optical networks and **allowing IP traffics to directly run on top of WDM channels. To do that, one of the most comprehensive solutions is to run packets directly on top photonic packet switches** as proposed by European carriers like BT and Alcatel. In facts, the photonic packet/cell switch research has recently become a very important research area. **Our work represents one of the few leading research works in the world in this area.**

The moment we proposed the work (1993), we have to take care the need of both an OTDM and a WDM networks. The technologies we developed here are useful for either approach. Basically, for each incoming packet/cell from all the optical channels, we need to align them in time before they entering the NxN space switch fabrics. A tunable optical delay line controlled by calculated electrical signals is needed. We may also need to change the information in the packet header before it leaves the switch and goes to the next node. The information could be the VCI in a system using the virtual-channel routing scheme or the packet delay in a burst switching system where the header is ahead of the packet payload. The delay between the header and the payload is changing at each node due to the add-on packet processing delay and the contention resolution delay. Before achieving both of the above functions (tunable delays and header information overwriting) an important function has to be performed and that is the cell or packet delineation function. The work is basically to identify the packet or cell boundaries from a stream of 1-0 optical signals. In a SONET system, the framing function is provided. When we run IP or cells directly on top of an optical channel, the cell or packet boundaries have to be identified.

Currently, there is basically no practical all optical logic devices. It is not hard to understand that electronic logic and control circuits has to be employed in this project to perform some critical operations. In our proposed switch, optical transparency is maintained everywhere to keep obtaining the advantages of the bandwidth and bit-rate as well as format independence. On the other hand, the intelligence is provided by the electronics. Since many of the functions at 2.5 Gb/s and above are not commercially available, we have to build them ourselves for the system demonstration. In this work, we have built 3 control circuit boards running at 2.5 Gb/s. These include a cell delineation circuit board, a VCI over-writing circuit board, and a cell synchronizer control circuit board. We also design and fabricate an 1x2 semiconductor optical amplifier (SOA) broadband space switch. Multiwavelength-signal switching using the fabricated switches is demonstrated. We also build the VCI overwriting and cell synchronization optical systems using

both LiNbO3 switches and the fabricated switches. We have completed the interfaces of the optical systems with the control circuit boards and finally demonstrated the proposed photonic ATM front-end processor at 2.5 Gb/s.

In the project, UMBC is responsible for the optical systems and Polytechnic University (Poly) is responsible for the electronic control systems. There has been many e-mails, phone calls, visits between the two campuses. Since Poly has only a 1 Gb/s testing system and UMBC has a 5Gb/s BER system, many testing works has to be first tuned to 1Gb/s at Poly and moved down to UMBC to be further tuned to 2.5 Gb/s before performing control functions. Poly researchers usually have to stay longer at UMBC to complete the interface and demonstration. The interaction among graduate students has created a great environment that neither campus can singly provide. Many exciting moments, ideas, problem solving discussions, and conference as well as journal papers have been generated through this process.

In the course of the research works, UMBC has graduated two M.S. students and two Ph. D. students (working at Bellcore, Cadence, E-Tek, and a cable TV equipment company at California) and Poly has two Ph. D. students just going to graduate. We have published 6 papers and filed 1 patent. More papers are in the process of preparation. Our works have drawn a great attention from many different equipment vendors and research organizations including NTT optical networking group, Alcatel, CSELT, New Bridge networks, ...etc.. The PI, Prof. Choa, was also visited by Cisco and invited by 3-Com to visit their head quarter and give an invited talk on our photonic packet switching research. In facts, a consensus has been reached by the optical communication community that fast photonic circuit switches and photonic packet switches will be the direction for the next generation optical network research.

A basic concept has formed after this research work. In an all-optical network cloud, photonic packet switches will be sitting everywhere in the middle of the cloud as backbone switches. Electronic buffered switches will be sitting on the edge of the cloud as edge switches to do format conversions and traffic regulation. Bursty traffics will be mostly buffered at the edge of the all-optical network and packets go to the same network address will be packed to large cells with a fixed length before send into the all-optical network. Inside the all-optical network, the backbone switches will handle fixed size cells all optically with fiber delay lines or loop memories. Since the traffics is relatively regulated, the buffer size requirement is more relaxed. Such a concept is now starting to be accepted by many industrial researchers. **As a leading research work in the world, our results can greatly contribute to the optical networking area and have impacts to the next generation Internet (NGI) and the global information infrastructure (GII).**

We summarize our special achievement in the following:

1. Cell delineation at 2.5 Gb/s. Currently, one of the best ideas to achieve IP on WDM may take the exactly same approach to delineate the IP packet boundary when the SONET framing is not available. We have achieved what many vendors just going to propose.
2. All optical cell header information exchange at 2.5 Gb/s. It is a very important function for future optical burst/packet switches.
3. All optical cell synchronization down to 100 ps resolution. Another very important function for future optical burst/packet switches.

Photonic ATM Front-End Processors

1. An Overview of The 3M Switch

The WDM ATM Multicast (3M) switch is an optically transparent ATM switch proposed by us. It combines the superiority of WDM and ATM techniques to provide a flexible and high-capacity switching function for the high-speed network. It takes advantage of photonics in large bandwidth and electronics in control and storage. The switch has a two-layer structure, where the ATM cell and its electrically converted routing header are split at the input port and then travel in parallel through an optical cell switching network and an electrical header processing and control network. The interconnection complexity of a switch fabric can be greatly reduced from $O(N^2)$ to O(N) by using the broadcasting and select scheme of WDM.

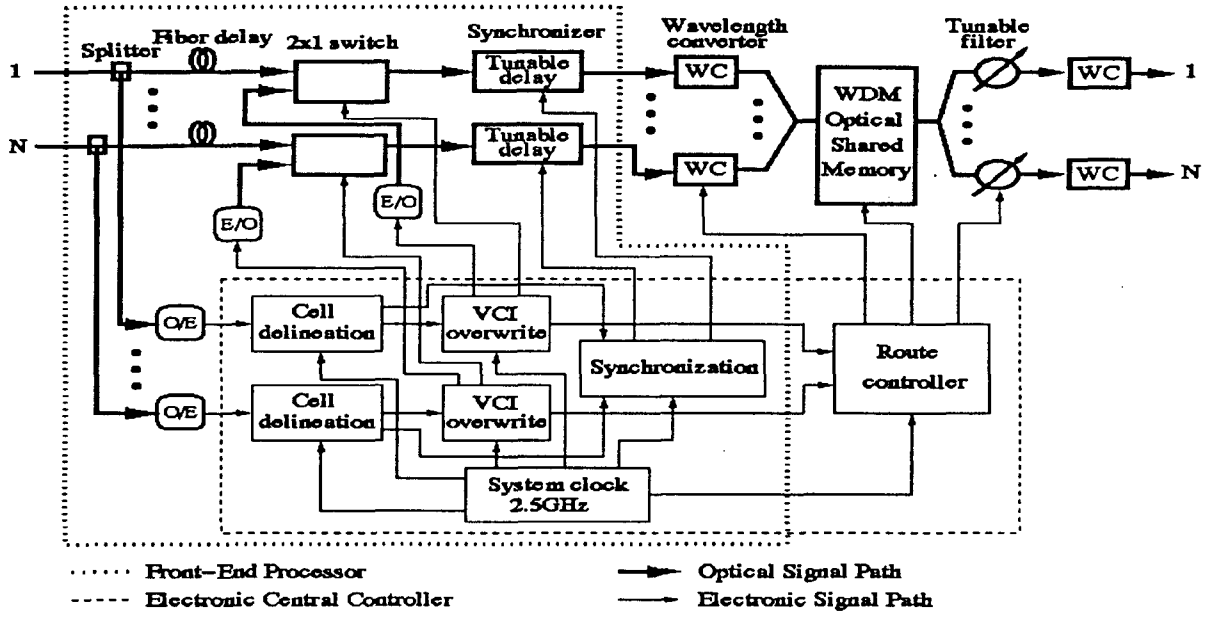


Figure 1 Architecture of the WDM ATM Multicast (3M) Switch

Figure 1 shows the architecture of an enhanced N × N 3M switch, where each port carries optical ATM cells at 2.5 Gb/s. The incoming data is split into two identical paths in each input port. One path remains in the optical domain through the switch, and the other is converted to an electronic format for header processing. Header processing performs table lookup and determines to which output ports the cells are routed. An electronic central controller, enclosed by a dashed line in Figure 1 performs the functions, such as cell delineation, VCI-overwrite controller, cell synchronization controller, and route controller. The first three are implemented in the in the front-end processor and are described in detail in this report. The route controller is being implemented to control the optical switch fabric, including wavelength converters, tunable filters, and a WDM optical memory. In the optical path side, after the synchronization and VCI overwriting, cells from each port will be wavelength-converted to different λ_i (i=1,...,N) by N wavelength converters and

sent to the WDM buffer memories to wait to be selected by the optical concentrators at the corresponding output ports. The WDM memories perform all optical buffering to temporarily store contented optical cells until the output port is available. These operations complete the switching and contention resolution functions of a share-memory switch. The final wavelength converter stage will shift cells to their preferred wavelengths.

2. The Architecture of The Photonic ATM Front-end Processor

The header of an ATM cell carries all the necessary information for routing. The photonic ATM front-end processor is designed to extract the cell header and perform the functions including cell delineation, VCI-overwrite, and cell synchronization. After phase alignment of incoming cells at each input port, they are sent to the optical shared memory of the switch fabric. Meanwhile, their routing information is passed to the router controller of the switch fabric. In the following, three basic units of the photonic ATM front-end processor are described in more detail.

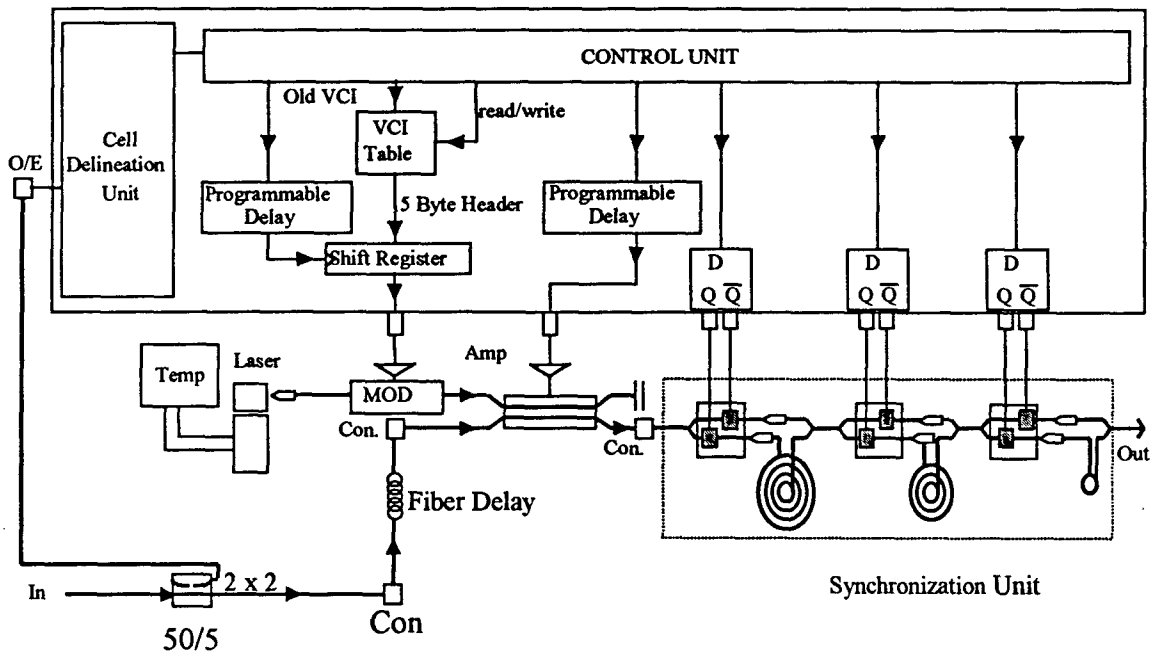


Fig. 2 Architecture of the Photonic Front-End Processor

Cell Delineation Unit

As shown in Figure 2, the optical cell stream is taped from each input line, converted to electronic format, and sent to the cell delineation unit. Cell delineation is a process used to identify the cell boundaries so that the incoming data stream can be further processed at the cell level by the following units, such as VCI-overwrite.

To search for the cell boundary, we adopted the standardized mechanism, checking of header error code (HEC). It takes advantage of the inherent Cyclic Redundancy Check (CRC) coding correlation between the cell header to be protected (the first 4 bytes) and HEC byte (the 5th byte of cell header). Initially, cell boundary is arbitrarily assumed and checked by performing a polynomial division bit by bit in the HUNT state. If the remainder (i.e., syndrome) for a complete calculation is zero, then this boundary is assumed to be correct. Otherwise, shift a bit from the data stream and repeat the procedure until the syndrome is zero. Once a cell boundary is primarily found, it has to be confirmed cell by cell for eight consecutive times in the PRESYNC state before the cell boundary is determined to be found. It then goes to the SYNC state. Once in the SYNC state, the cell boundary is claimed to be lost when seven consecutive mismatches occur. As a result, the above procedure for cell delineation will start all over again (from the HUNT state).

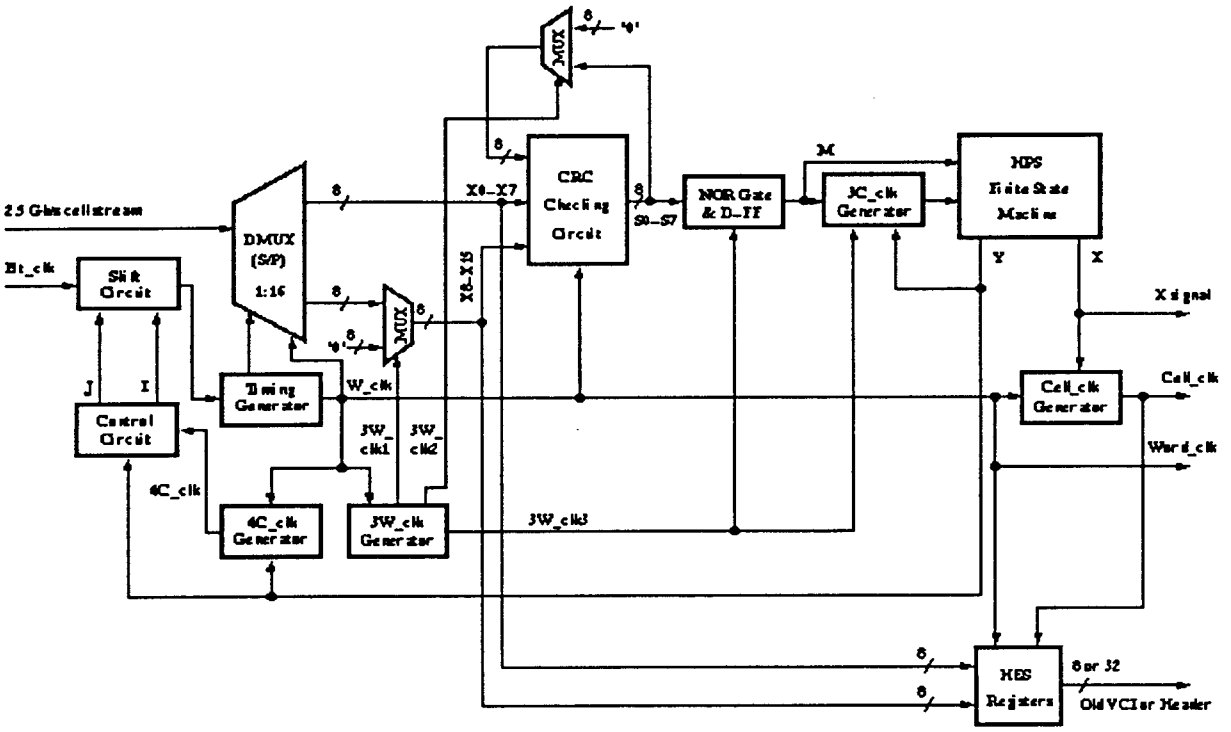


Figure 3 Block Diagram of the Cell Delineation Unit

As shown in Figure 3, in order to relax the high-speed circuit requirement, the serial bit stream (2.5 Gb/s) is first converted to 16-bit parallel words (155 Mb/s) through a serial to parallel converter. A 16-bit parallel format of CRC checking circuit is used to perform polynomial division and the syndrome is checked every three word clock cycle. A HPS (HUNT, PRESYNC, and SYNC) finite state machine is used to perform the state transition between HUNT, PRESYNC, and SYNC states, as mentioned above. If a syndrome equals zero, then the finite state machine goes to PRESYNC from HUNT state and disables a set of control and shift circuits by a signal Y. Otherwise, the finite state machine informs the control and shift circuits to inhibit a bit and a byte every three cell clock cycle. Once the cell boundary is confirmed, the state machine goes to SYNC state and sends a signal X to create a cell clock, which indicates to the location of the cell boundary

that is found. The cell clock and signal X are passed to the VCI-overwrite unit together with the old VPI/VCI and the word clock.

VCI-overwrite Unit

Once cell boundaries are recognized and confirmed by the cell delineation unit, the state machine moves to the SYNC state and enables the VCI-overwrite unit with the cell clock and signal X, as shown in Figure 4. The main function of this unit is to overwrite the VPI/VCI field of the incoming cell header in the optical domain. The VCI-overwrite unit performs the table lookup in the electronic domain, converts the new VPI/VCI to optical format, and replace the old values by using a 2 × 1 optical switch. The challenge is how to handle this high-speed overwriting because each bit is only 400ps at the bit rate of 2.5 Gb/s. We solve it by (a) replacing the whole cell header instead of just only the VPI/VCI fields, and (b) using electronic variable delay lines (programmable delay) to compensate for the time difference between the old header and the new header.

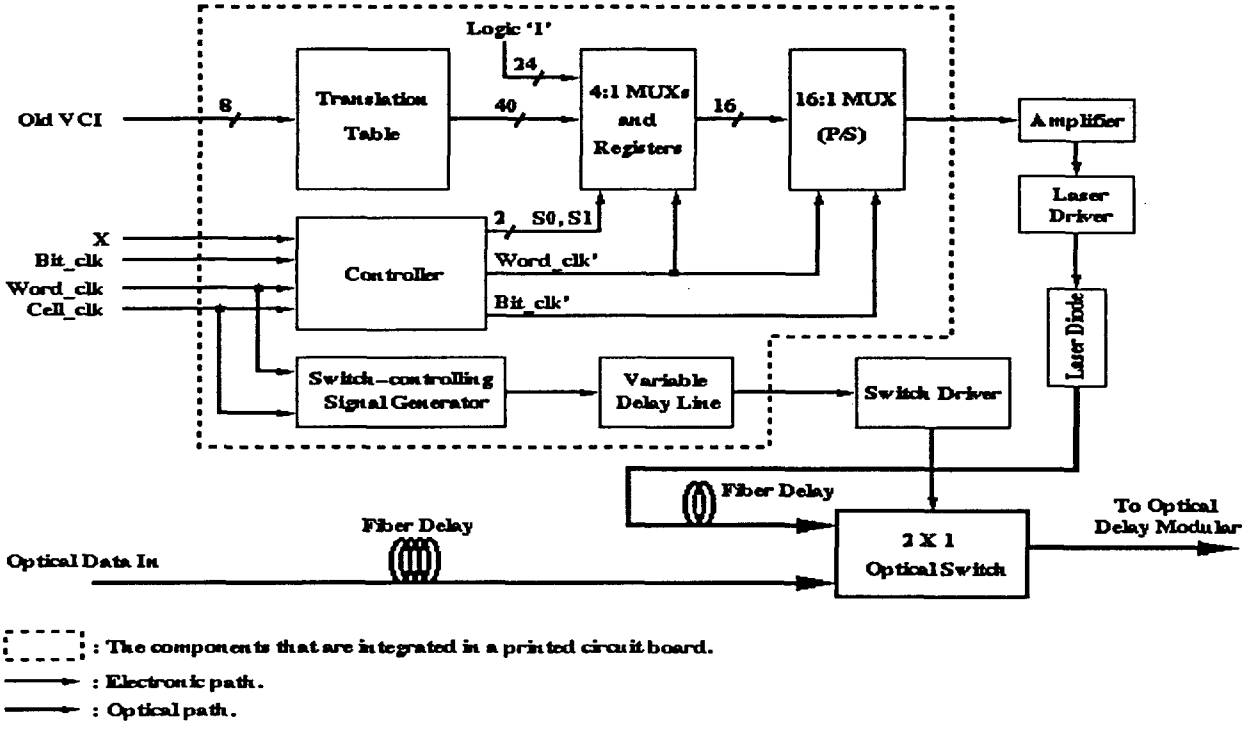


Figure 4 Block Diagram of the VCI-overwrite Unit

As shown in Figure 4, the new header is obtained by table lookup and then converted to serial format by a parallel to serial converter. Then, it is used to control a laser driver to drive a DFB laser diode that generates the cell header in the optical domain. The new header replaces the old one using a 2 × 1 optical switch that is controlled by a switch-controlling signal generator with 6 bytes of pulse in every cell time slot. The successfully overwritten cells are sent to fiber delay lines in the cell synchronization unit.

Cell Synchronization Unit

The cell synchronization unit is used to optically align cells from different inputs to the extent of 1/4 bit (100 ps or 2 cm optical delay line at 2.5 Gb/s) before they are further sent to the switch fabric. Because of this timing requirement, we divided our control system into two parts. A coarse adjustment circuit is used to control the first nine stages of the optical delay element up to 1 bit, and a fine adjustment circuit is used to control the last two stages up to 1/4 bit. Each stage of the optical delay element consists of a splitter, a combiner, two semiconductor optical amplifier (SOA) gates, and a different length of fiber delay line $T/2^n$ (where T is one cell time and n is from 1 to 11). Figure 5 shows the functional block diagram of this unit.

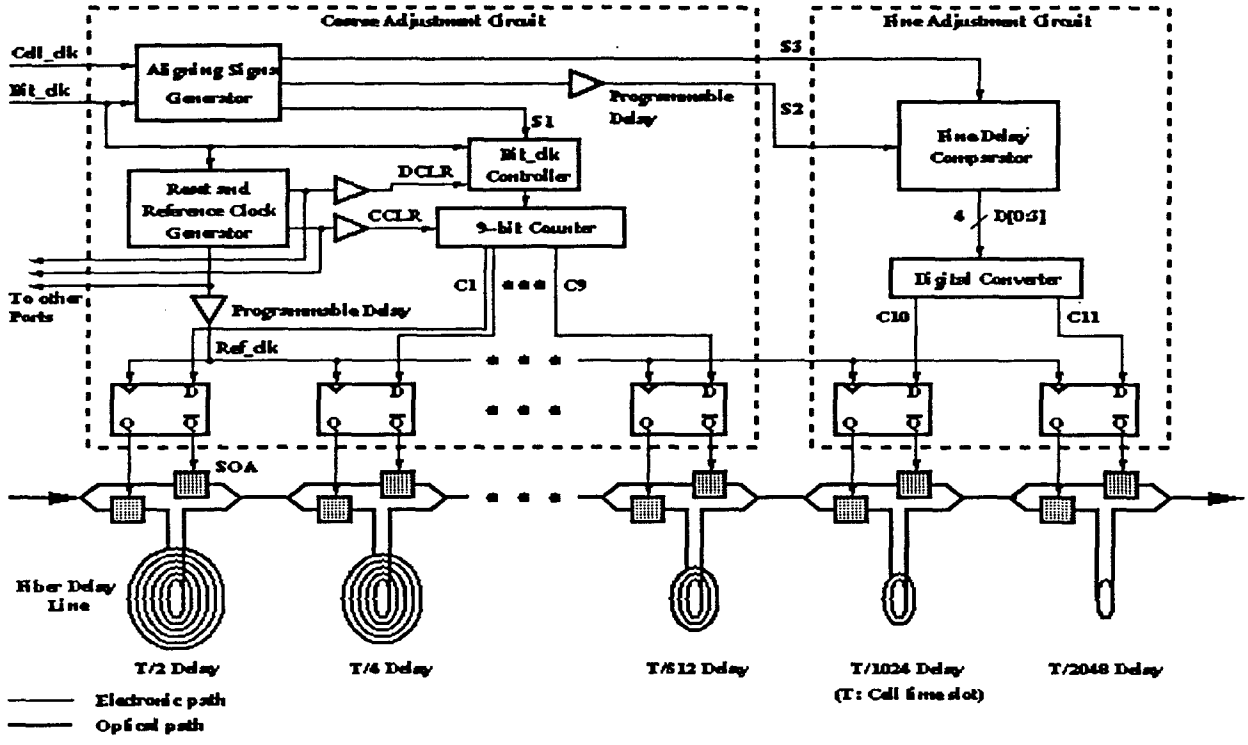
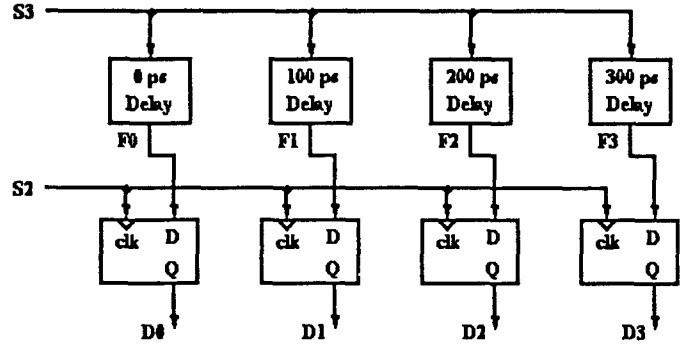


Figure 5 Block Diagram of the Cell Synchronization Unit

As mentioned before, the cell clock generated in the cell delineation unit can be used to indicate the real location of the cell boundary. Therefore, by comparing this cell clock to a reference clock generated by the system, a 9-bit digitized timing difference (up to one bit level) can be obtained by using a 9-bit counter in the coarse adjustment circuit. Each binary digit (C1 to C9) is used to control the switching at the two SOA gates, to determine if each cell passes or does not pass the fiber delay line, in one of the first nine stages of the optical delay system.

However, to identify the timing difference for less than one bit is challenging. A novel sampling technique is adopted to avoid using a 10-GHz clock to adjust the phase down to 100 ps. Figure 6 shows the circuit, which adjusts signal S3 (related to cell clock) into four kinds of phase

differences by delaying 0, 1/4 bit (100 ps), 1/2 bit (200 ps) and 3/4 bit (300 ps). Signal S2 (related to bit clock) is used to sample these four different phase-delayed signals to get four sampled signals, [D0, D1, D2, D3]. By converting them into two digits, C10 and C11, according to the conversion table shown in Figure 5, we can use them to control the SOA gates of the last two stages of the optical delay system.



(a) Fine Delay Comparator

C10	C11	D0 (0ps)	D1 (100ps)	D2 (200ps)	D3 (300ps)
0	0	0	0	0	0
0	0	1	0	0	0
0	1	1	1	0	0
1	0	1	1	1	0
1	1	1	1	1	1

(b) Conversion table between [C10,C11] and [D0,D1,D2,D3]

Figure 6 Fine Delay Comparator and a Table Conversion

With different combinations of C1 to C11, all stages of optical delay elements are tuned to the desired delay needed to compensate and align the phase of incoming cells. For example with [C1, C2, ..., C11] = [1, 0, 1, 0, 0, 0, 0, 0, 0, 0, 1], a total delay of $T/2 + T/2^3 + T/2^{11}$ (the last term is 1/4 bit) , is added by the cell synchronization unit.

3. Implementation and Testing

In this section, we described in detail the architectures of three basic units of the photonic ATM front-end processor. Their implementation and testing results are described in this section.

3.1 Implementation

In order to implement the photonic front-end processor operating at 2.5 Gb/s, we use off-shelf ECL or GaAs chips to implement the three basic units in three printed circuit boards (PCBs). We used Mentor Graphics's Design Architech to design the circuits and Quicksim II to simulate and check the circuits. We then used Borad Station, including Librarian, Package, Layout, and Fablink, to design the PCBs. Since the operation frequency of the PCBs is at 2.5 GHz, the wiring layout is done manually to ensure the delay skew is minimized. Note that each bit has only 400 ps. These PCBs are fabricated by Multilayer Technology. The boards were first tested at 1 Gb/s at Polytechnic University due to the speed limitation of the instruments. They were then integrated with optical subsystems at the University of Maryland, Baltimore County, and tested to function correctly at 2.5 Gb/s.

Cell Delineation Unit Board

Figure 7 shows the PCBs of the cell delineation and VCI-overwrite units. The components we used are mostly Motorola's ECLinPs Family ICs and small quantities of NEL's SST ECL Logic ICs and GaAs ICs. The NEL's GaAs ICs outperforms all ECL ICs in speed characteristic, but are more expensive. They are only used in the shift circuit of the feedback part, as shown in Figure 3 (file: cl.eps), where we need to inhibit a bit from bit_clk and shift a bit in case the assumed cell boundary is incorrect. In addition, a Vitesse's 16-bit demultiplexer (VS8062) is used to perform serial to parallel conversions. This chip converts a 2.5 Gb/s serial bit stream to 16-bit parallel words at 155 Mb/s. The advantages of parallel conversion are to reduce the number of high-speed components and implementation costs, and to simplify the design and testing of circuits.

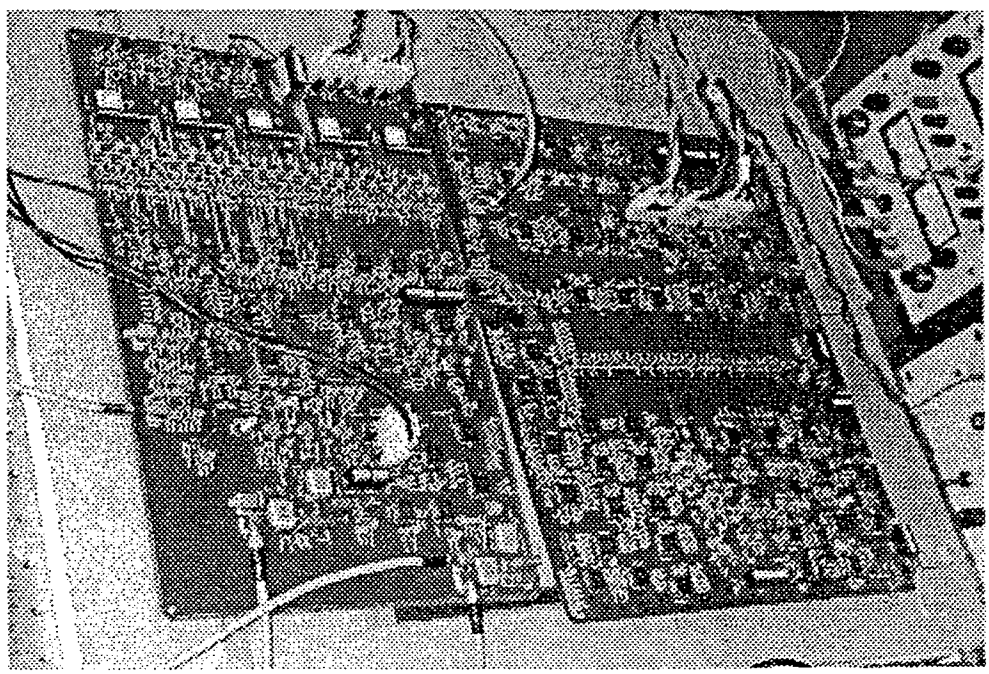


Figure 7 The PCBs of the Cell Delineation and VCI-overwrite Units

In addition to selecting suitable chips to meet our high-speed requirement, the high quality of the PCB material (Getek) is used to meet the high-speed requirement. The impedance of the interconnection wires is 50 ohms. The PCB has 8 layers and its the physical size is 15 × 13 inches. Figure 7 summarizes the characteristics of these PCBs.

Electronic Controller of VCI-overwrite Unit Board

We use a few CMOS chips, Atmel's EPROMs (AT27C256R), on this PCB to store the translation table information. Instead of using RAM (random-access memories) chips with a microprocessor to update the table dynamically, the EPROM chips are used to simply the design. In addition, a Vitesse's 16-bit multiplexer (VS8061) was used to perform the parallel to serial conversion for the cell headers, which are further converted to optical format to replace the old header values. The characteristics of board are shown in Figure 8.

Board Name	Cell Delineation	VCI–Overwriting	Cell Synchronization
Size (inch)	15 x 13	15 x 10	15 x 20
Number of Layers	8	7	10
Material	Getek	Getek	Getek
Maximum Operation Speed	2.5 Gb/s	2.5 Gb/s	2.5 Gb/s
Power (watt)	40	25	41
Number of IC	95	94	61 + 36/N †
Components	Motorola's ECLinPS Family NEL GaAs IC NEL SST ECL Logic IC Vitesse's MUX/DMUX GaAs IC Atmel's AT27C256R EPROM		

† There are 36 chips in Reset and Reference Clock Generator that are shared by all ports (N).

Figure 8 Summary of the Printed Circuit Boards

Electronic Controller of Cell Synchronization Unit Board

Because of the need to align the incoming cells to the extent of 1/4 bit, choosing proper components is very crucial. For example, to determine the timing differenceless than one bit between cell and Ref_clk in fine delay comparator, as shown in Figure 7 (file: fcc2.eps), D flip-flops with low setup and hold time are required. Motorola's differential data and clock D flip-flop (MC10EL52) meets this requirement with zero setup time and 50 ps hold time. In addition, we used

several Motorola's programmable delay chips (MC10E195) to adjust and compensate for the timing of several signals in the coarse and fine adjustment circuits. The typical chip delay is variable and ranges from 1390 ps to 3630 ps with about 20 ps delay step resolution.

The reset and reference clock generator, which is shown in the coarse adjustment circuit in Figure 5, is shared by all input ports in the 3M switch.The PCB has 10 layers and its physical size is 15 × 20 inches. Other characteristics of the board are shown in Figure 8 (file: bsummary2.eps).

All the optical devices and subsystems in the photonic ATM front-end processor, such as SOA gates, laser diode, and 2 × 1 optical switch, VCI overwriting optical unit, and multistage cell synchronizer optical unit are developed and provided by University of Maryland, Baltimore County. The work are described in the following.

1x2 SOA Switches:

In the course of fabricating the integrated 1x2 Y-junction SOA switch we have gone through several generations of devices. Although for each different device generation the performance is always getting improved, the process is effort and material consuming. Fortunately, through the relationship with AT&T Bell Labs. (and later on Lucent Bell Labs.), our projects were firmly supported by their crystal growth efforts. In the following we report the detailed fabrication processes of the work.

In the first generation Y-junction semiconductor optical amplifier (SOA) gate switches. The active section has a buried heterostructure (BH) and the passive section has a buried rib structure. When we do the BH deep etch we have to protect the passive section with a thick photoresist. Since there is no etching activity in the passive side, the acid is very dense and the etching speed is very fast near the boundary of the active section than that near the center of the active section. The much faster undercutting etching can easily break the waveguide near the active boundary. The yield was low at that moment.

In our second generation switch and our 10-stage cell synchronizer designs, we have corrected the problem by using masks with wider stripe width near the active/passive junctions. We then completed the fabrication of both the second generation switches and the first generation of an integarted 10-stage cell synchronizers. An integrated 3-stage cell synchronizer are shown in Fig. 9. A bonded and a chip of the Y-junction SOA gate switch is shown in Fig 10.

In the second generation SOA gate switches we have overcome the non-uniform etching problem and successfully fabricated and demonstrated on/off operations of the switch. However, when we were trying to couple light into fibers from those devices, the distance between waveguides became an issue. The standard distance between waveguides was 508 μm before. It just changed to 250 μm and its multiples at that moment. We found later that we can commercially obtain lensed fiber arrays made of silicon v-grooves with standardized (250 μm) distance between fibers. We also found that to couple light in and out of a semiconductor passive waveguide is extremely difficult. Adding active sections to both the inputs and outputs of a semiconductor chip is very helpful.

Based on the findings, we designed and fabricated our 3rd generation devices as shown in Fig. 11. The distance between the 2 output waveguides are exactly 250 μm. The active sections on each input and output waveguides are 400 μm long. We can easily build a multi-stage cell synchronizer using an array of such switches as shown in Fig. 12. The final size of the device can be much smaller than the previous 10-stage cell synchronizers. Packaging can also be simplified from doing 3-side fiber alignment to that of two-side fiber alignment. Fig. 13 shows the switching characteristics of the third generation Y-junction SOA gate switches. The fall time is fast due to the stimulated emission. The rise time is limited by the Auger recombination rate around 1 ns and can be reduced if the switching current is increased. **A very interesting application of the photonic space switch is its capability to switch multiwavelength signals with one single switch and in one switching operation**. A word of 64-bit information can be direct to different locations with one fiber, one switch and one switching operation. On the other hand, the same task will require 64 connections and 64 electronic switches on operation. The extra wavelength domain of photonics can greatly reduce the complexity and cost of interconnects. We have experimentally demonstrated a new generation switch, the data block switch, which can direct a full block of parallel data to a desired location. The experiment setup for the data-block switching is shown in Fig. 14. The SOAs have very broad gain profile covering more than 50 nm as shown in Fig.15 (a). The multi-wavelength light signals, with 7 of them near 1550 nm (separated by 100 GHz spacing) and one at 1553 nm, are coupled into an 8x1 optical coupler and launched into the switch. Fig. 15 (b) shows the multiwavelength spectrum. A tunable filter at the switch output is used to select signals to observe the switching results at each particular wavelength. Fig. 15 (c) and (d) shows the switched "1010" signal streams at 1553 nm and 1533 nm respectively. The "1" and "0" can be clearly identified when the switch is tuned "ON" and the background of the "OFF" state is clear. Very good contrast ratio is obtained and there are very little differences between the received signals and at the two extreme wavelengths.

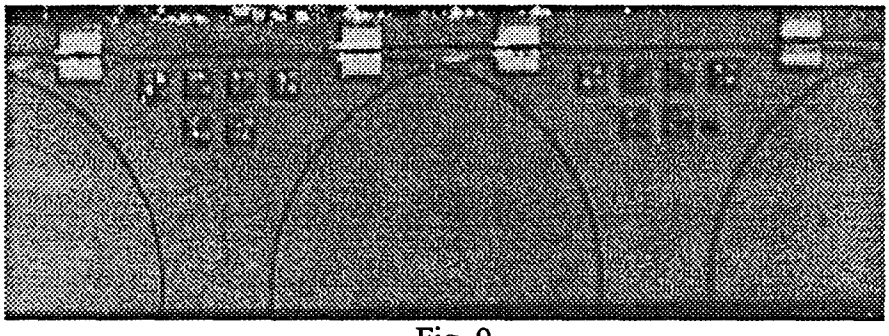


Fig. 9

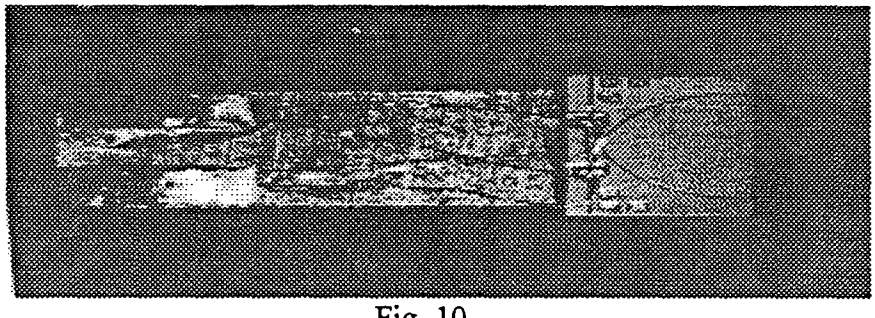


Fig. 10

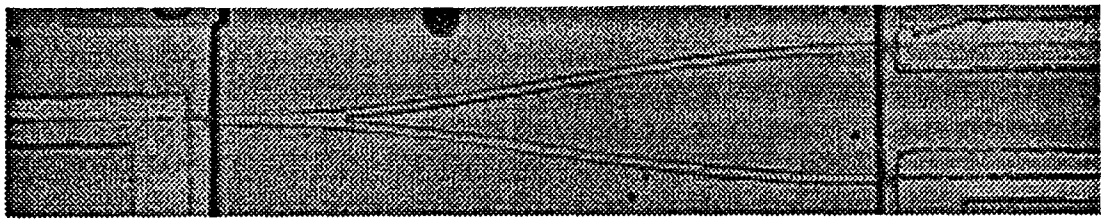


Fig. 11 A fabricated 1x2 SOA gates switch

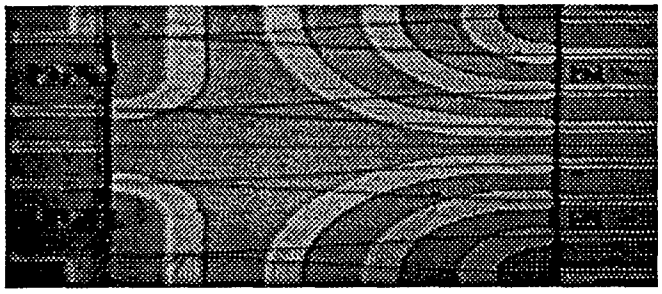


Fig. 12 Integrated Cascade multistage 1x2 switches

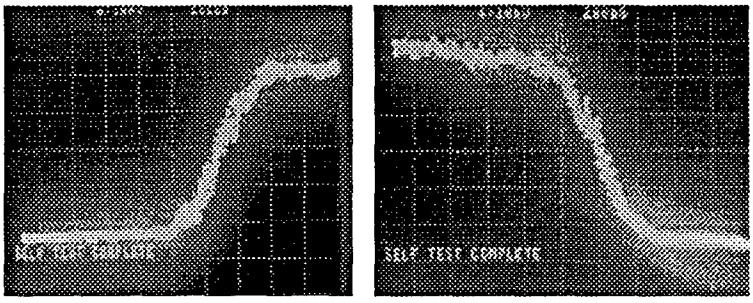


Fig. 13. Switching characteristics of an SOA switch (200 ps/div.).

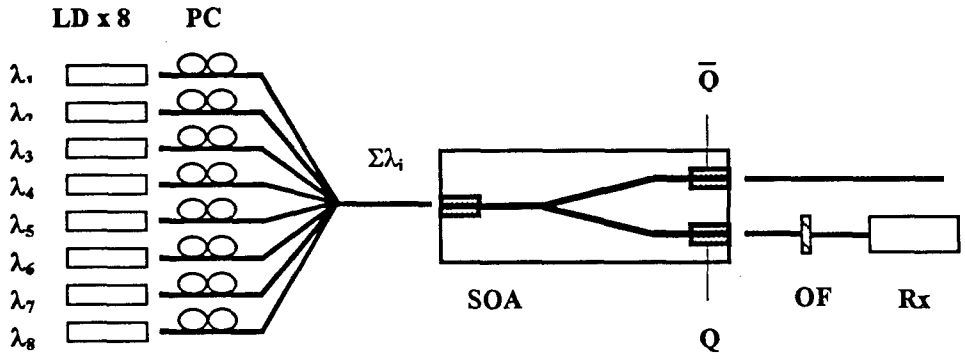


Fig. 14 Experimental setup. PC: polarization controller, OF: optical filter, LD:

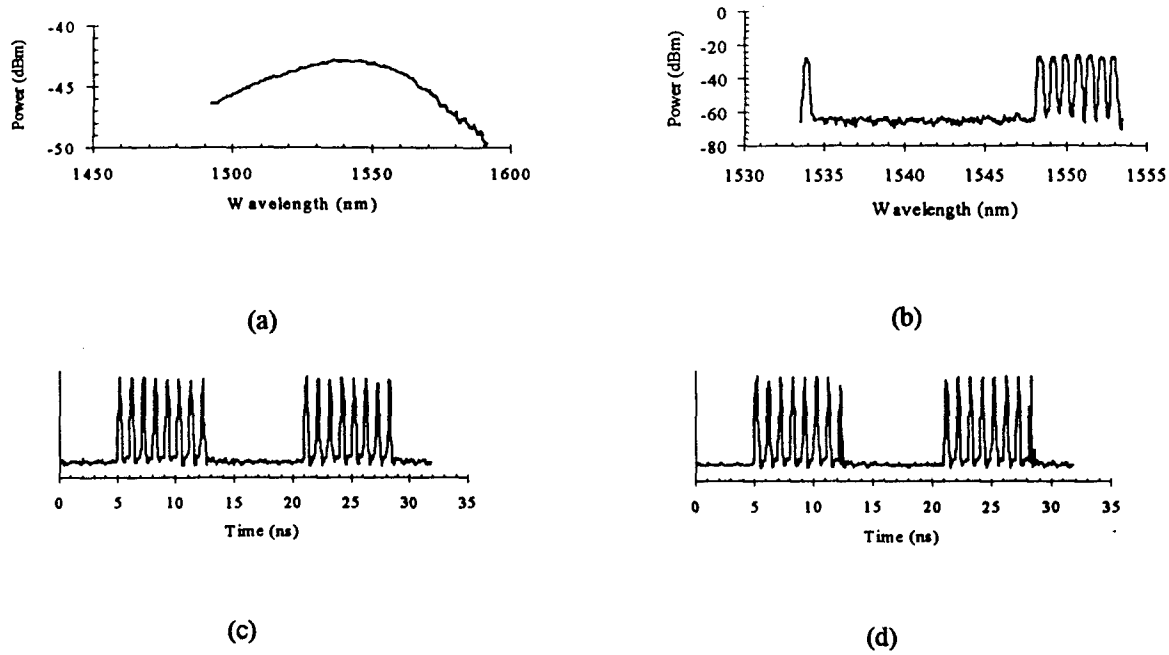


Fig. 15. (a) The SOA gain profile. (b) Multiwavelength signals. (c) Switched "1010" data streams at 1553 nm. (d) Switched "1010" data streams at 1533 nm.

3.2 Testing

To validate the design and implementation of the whole system, a series of testing process is necessary. The testing is divided into two parts. One involves the cell delineation and VCI-overwrite units. The other involves only the cell synchronization unit.

Testing of Cell Delineation and VCI-overwrite Unit

We integrated two PCBs (cell delineation and VCI-overwrite units) with the necessary optical devices as shown in Figure 16. A data generator generates the 2.5 GHz Bit_clk and a series of 2.5 Gb/s back-to-back cells. These test cells have 64 bytes with 5 bytes of header, 48 bytes of payload, and two sections of guard times (logic `1'), which are 6 and 5 bytes, respectively,

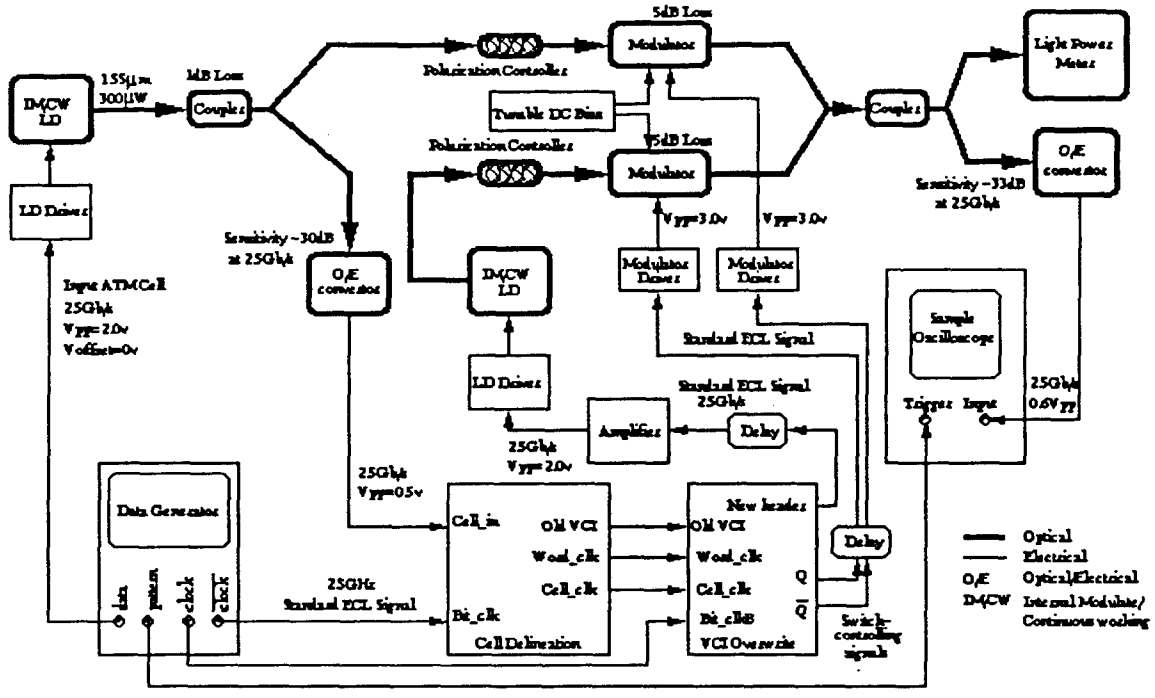


Figure 16 Testing Setup of the Cell Delineation and the VCI-overwrite Units

as shown in Figure 17. The reason for inserting the guard time is to compensate for the slow switching of optical devices, for example, optical tunable filters, which are used in the switch fabric in the 3M switch. To simplify the testing, the test cells have a random payload but an identical cell header pattern, which is {00001010, 11001100, 11101110, 11110000, 10100000}. We assumed that only the third byte (representing VPI/VCI) and fifth byte (HEC byte) are updated in the VCI-overwrite unit.

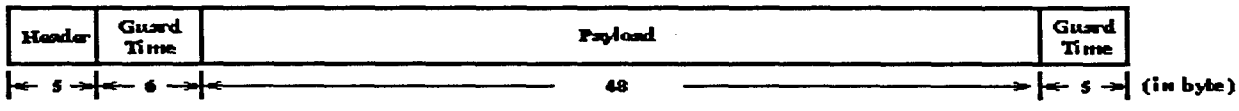


Figure 17 Cell Format in Our Design

Since inputs and outputs of two PCBs have standard ECL voltage levels, with V_{pp} = 0.9 V, which is different from that of the laser driver (V_{pp} = 2.0 V), an amplifier is thus needed. The 2 × 1 optical switch is accomplished by two modulators and their drivers controlled by the electronic controller of the VCI-overwrite unit. A high-speed oscilloscope is used to analyze the over-written cell stream, which is converted from optical format to electronic format by an O/E converter.

When the system powers on, the data generator provides a cell stream and the Bit_clk to the system. Depending on the position of the first cell boundary selected by the cell delineation unit, the correct updated cells can be obtained and monitored in the oscilloscope within 15 nsec.

Figure 18 shows the testing result of cell delineation and VCI-overwrite units. The new header becomes {00001010, 11001100, 00010001, 11110000, 01110111}, which meets our expectation.

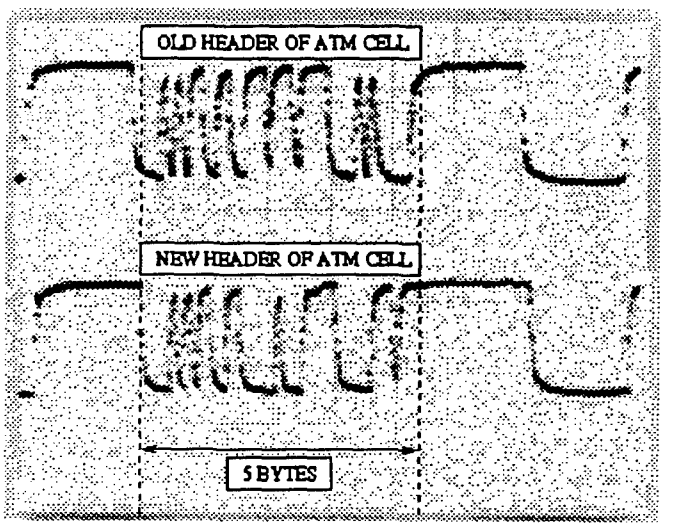


Figure 18 Testing Result of the Cell Delineation and VCI-overwrite Units

Synchronization Testing of Cell Unit

We have built a PCB that includes all 11 stages of optical delay elements. The required delay is generated as a control word to turn on or off each 1x2 semiconductor optical amplifier (SOA) Y-junction switch like a toggle switch (delay or not delay). The fiber delay length varies from 1/2, 1/4, ... to $1/2^n$ of an ATM cell. The synchronizer accuracy can be as small as $1/2^n$ of one cell period, where n is the number of delay stages. Fig. 19 demonstrate the 1/8, 1/4, and 1/2 packet delay by using appropriate fiber length for an optical packet with 400 ns length at 2.5 Gb/s. The fiber to fiber insertion loss of the SOA switch is currently at 5 dB. It achieved a very good contrast.

Since the most difficult in aligning the phase is the last few stages, we also demonstrate the phase alignment of the last three stages to prove the function of the cell synchronization unit. A reference clock is distributed in the whole switch system and used by all inputs as a common alignment basis. The electronic part of the unit has correctly operates at 2.5 Gb/s and is being integrated with optical devices for complete testing. The generated optical delays as small as 100 ps were achieved. Fig. 20 (a), (b), (c), and (d) show the delays generated from 100 ps to 400 ps. The accuracy can be as small as an ¼ bit at 2.5 Gb/s.

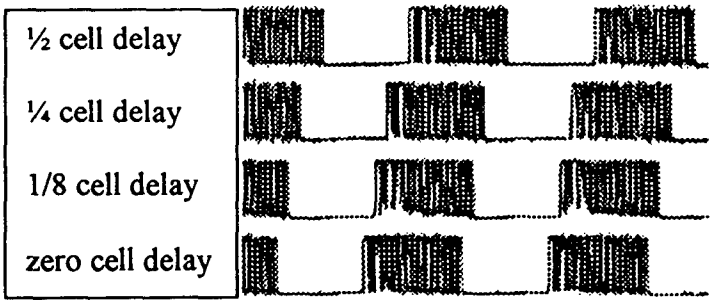
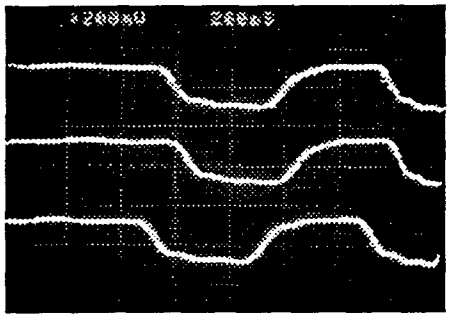
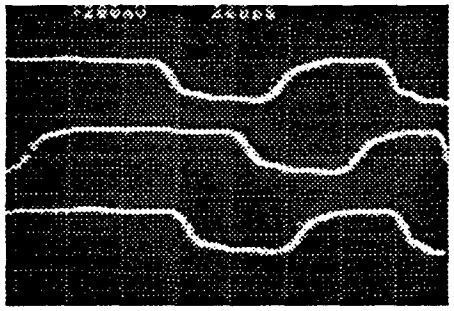


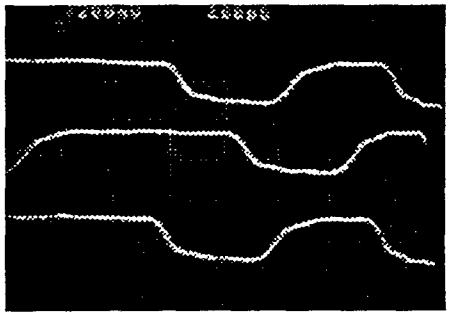
Fig. 20. Coarse Delays Adjustment



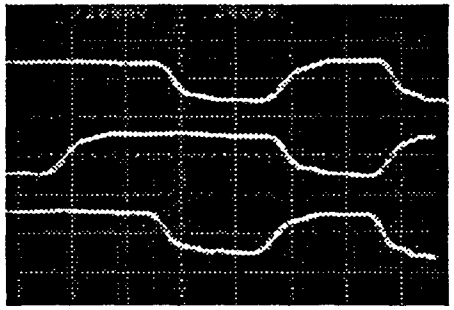
(a) Delay Resolution: 100 ps



(b) Delay Resolution: 200 ps



(c) Delay Resolution: 300 ps



(d) Delay Resolution: 400 ps

Fig. 20. Fine Delay Adjustments

4. Status of Efforts:

At this stage we have completed all our efforts of the "photonic ATM front-end processors" project. We built systems and demonstrated cell delineation, VCI overwriting, and cell synchronization operations at 2.5 Gb/s. The results are very useful for the construction of near future photonic burst switches and photonic packet switches for NGI and GII applications.

5. Multidisciplinary Education:

In the course of the research works, there has been many e-mails, phone calls, visits between the two campuses. The interaction among graduate students and postdocs has created a great environment of multidisciplinary discussions and. Many ideas, problem solving discussions, and research papers have been generated through this process. UMBC has graduated two M.S. students and two Ph. D. students and Poly has two Ph. D. students just going to graduate. We have published 6 papers and filed 1 patent in this area. More papers are in the process of preparation. In the last week's European Conference on Optical Communication (ECOC'98, Sep. 21-25, 1998) we have present two papers describing part of our complete switch research works. Our works have drawn a great attention from many different equipment vendors and research organizations including NTT optical networking group, Alcatel, CSELT, New Bridge networks, ...etc.. Our constant supporter, Lucent Technology has also shown a great interest in what we are doing. The PI, Prof. Choa, was also visited by Cisco and invited by 3-Com to visit their head quarter and give an invited talk on our photonic packet switching research. We list in the following the project supported personnel, the interaction/transition, and publications as well as patent applications.

Personnel Ever Supported:

1. UMBC:
   - **a. Faculty**:
   - Professor F. S. Paul Choa, Overall project
   - **b. PostDocs**:
   - Dr. X. Wang, (1/2 time) Device Processing
   - Dr. Y. Chai, (1/2 time) System Experiment
   - **c. Graduate Student**:
   - **M. S. Students**:
   - B. G. Gopal: (geaduated) is now working at Cadence Semiconductor at CA.
   - J. Busrur: (graduated) is now working at Bellcore, NJ.
   - **Ph. D. Students**:
   - M. H. Shih: (graduated) is now working at SVIC, CA, a cable TV lightwave eqp. Co.
   - J. H. Chen, (graduated) is now working at E-Tek, CA. At a new photonis switching branch.
   - J. Y. Fan (to be graduated at Dec. 1998) Device fabrication and characterization.
   - L. Wang: system integration.
2. Polytechnic University:
   - **a. Faculty**:
   - Professor H. Jonathan Chao, Electronic control unit, system integration.
   - **b. PostDoc**:
   - Dr. Zhijian Zhang (1/2 time) and Dr. Liji Wu. (1/2 time)
   - **c. Graduate Student**:
   - Mr. S. H. Yang, (to be graduated at Dec. 1998) Circuit design.
   - Mr. T. S. Wang, (to be graduated at Dec. 1998) Architecture.

Interaction/Transitions:

1. We have been continuously working together with researchers at Lucent Technology to develop photonic switching technologies. Lucent's research executive director, Dr. Bill Brinkman and director, Dr. A. M. Glass feel interested in the project we are doing and are very supportive to the work for the last 3 years.
2. We have been contacted by 3-Com, CA. about our photonic device capability and photonic switch works. 3-Com is particularly interested in our photonic ATM switches. People in their Israel factory (Fab. ATM switches) has found from the web about our work and 3-com has invited the PI Prof. Choa to visit their research headquarter at San Jose and give an invited talk there.
3. We are also in the process to try to commercialize our photonic devices. Interested parties include LCcore at MD, Finisar at CA, and Cisco at CA. Cisco people have also visited UMBC and is going to have more interactions later.

Publications:

1. J. H. Chen, X. Zhao, and F. S. Choa, "Design consideration of semiconductor optical amplifier linearity," IEEE LEOS Annual Meeting, paper TuX5, 1997.
2. X. Zhao, J. H. Chen, F. S. Choa, "Performance analysis of gain-clamped semiconductor optical amplifiers using different clamping schemes," IEEE LEOS Annual Meeting, paper TuY4, 1997.
3. J. Fan, J. P. Zhang, Y. Chai, F. S. Choa, P-. L. Liu, T. Tanbun-Ek, P. Wisk, W. T. Tsang, G. Zydzik, C. A. Burrus, "Electrical control optical delay lines made of Y-junction SOA switches," Conference on Lasers and Electro-Optics and International Quantum Electronics Conference Proceeding, San Francisco, paper CThO44, 1998.
4. J. Y. Fan, X. Zhao, J. P. Zhang, F. S. Choa, Y. Chai, J. H. Chen, E. Miller, H. Motteler, P. -L. Liu, T. Tanbun-Ek, P. Wisk, W. T. Tsang, G. Zydzik, C. A. Burrus "Wavelength-division-multiplexed (WDM) data block switching for parallel computing and interconncet", SPIE, International Conference on Applications of Photonic Technology, Ottawa, Ontario, Canada, July, 1998.
5. J. Y. Fan, L. M. Wang, Y. Chai, F. S. Choa, H. J. Chao, Z. Zhang, L. Wu, S. Yang, "A photonic ATM front-end processor", Proc. ECOC'98, paper TuB27, 1998.
6. H.J.Chao, Z. Zhang, L. Wu, S.H. Yang, F.S. Choa and L. Wang," A photonic ATM front-end processor", IEEE Proc. LEOS'98 Annual Meeting, paper WR3, 1998.
7. H. J. Chao, L. Wu, Z. Zhang, S. H. Yang, L. M. Wang, Y. Chai, J. Y. Fan, J. P. Zhang, F. S. Choa, "A 2.5 Gb/s optical ATM cell synchronizer", Submitted to OFC'99.

Patent Filed:

F. S. Choa, "Wavelength-Division-Multiplexed data-block switching", 1998. (pending)